AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended): A semiconductor device, comprising:

a well of a first conductive type formed in an upper layer of a substrate;

a low-concentration layer of the first conductive type having a lower impurity concentration than the well, the low-concentration layer being formed in an extreme surface layer of a channel portion of the well;

a high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film, the high-k gate dielectric layer being formed on the low-concentration layer;

a gate electrode formed on the high-k gate dielectric layer; ~~and~~

extension regions of a second conductive type formed in an upper layer of the well, the extension regions sandwiching the low-concentration layer; and

source/drain regions of ~~a~~ the second conductive type formed in an upper layer of the well, the source/drain regions sandwiching the low-concentration layer and the extension regions; wherein

a depth of the low-concentration layer from an upper surface of the substrate is smaller than a depth of the extension regions from the upper surface of the substrate.

Claim 2 (currently amended): A complementary semiconductor device having a n-type circuit region and a p-type circuit region, comprising:

a p-type well formed in an upper layer of a substrate of the n-type circuit region;

a n-type well formed in an upper layer of the substrate of the p-type circuit region;

a p-type low-concentration layer formed in an extreme surface layer of a channel portion of the p-type well, the p-type low-concentration layer having a lower impurity concentration than the p-type well;

a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well, the n-type low-concentration having a lower impurity concentration than the n-type well;

a high-k gate dielectric layer formed on the p-type and n-type low-concentration layers, the high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film;

a gate electrode formed on the high-k gate dielectric layer;

n-type extension regions formed in an upper layer of the p-type well, the n-type extension regions sandwiching the p-type concentration layer;

n-type source/drain regions formed in an upper layer of the p-type well, the n-type source/drain regions sandwiching the p-type low-concentration layer and the n-type extension regions; ~~and~~

p-type extension regions formed in an upper of the n-type well, the p-type extension regions sandwiching the n-type low-concentration layer; and

p-type source/drain regions formed in an upper layer of the n-type well, the p-type source/drain regions sandwiching the n-type low-concentration layer and the p-type extension regions; wherein

a depth of the p-type low-concentration layer from an upper surface of the substrate is smaller than a depth of the n-type extension regions from the upper surface of the substrate; and

a depth of the n-type low-concentration layer from the upper surface of the substrate is smaller than a depth of the p-type extension regions from the upper surface of the substrate.

Claims 3-5 (canceled).

Claim 6 (new): The semiconductor device according to claim 1, wherein the depth of the low-concentration layer from the upper surface of the substrate is smaller than about 10 nm.

Claim 7 (new): The complementary semiconductor device according to claim 2, wherein the depth of the p-type low-concentration layer from the upper surface of the substrate is smaller than about 10 nm; and

the depth of the n-type low-concentration layer from the upper surface of the substrate is smaller than about 10 nm.